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## The upgraded HADES trigger and data acquisition system

HADES collaboration,

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**ABSTRACT:** The HADES experiment is a High Acceptance Di-Electron Spectrometer located at GSI in Darmstadt, Germany. Recently, its trigger and data acquisition system was upgraded. The main goal was to substantially increase the event rate capability by a factor of up to 20 to reach 100 kHz in light and 20 kHz in heavy ion reaction systems. The total data rate written to storage is about 400 MByte/s in peak.

In this context, the complete read-out system was exchanged to FPGA-based platforms using optical communication. For data transport a general-purpose real-time network protocol was developed to meet the strong requirements of the system. In particular, trigger information has to reach all front-end modules with latencies of less than 5  $\mu$ s through up to 10 intermediate hubs in a star-like network setup. Monitoring and slow control features as well as readout and trigger distribution

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were joined in a single network protocol made up by three virtual channels with inherent arbitration by priority and a typical switching time of 100 ns. The full DAQ system includes about 550 FPGAs distributed over the complete detector system. For control and monitoring a virtual address space spanning the whole network is provided. Data are merged by the network hubs into data streams and passed on to a server farm using an Ethernet infrastructure. Due to the electromagnetic noise environment, several transmission error detection and correction features were included.

In collaboration with groups from experiments of the FAIR accelerator complex, further developments based on the versatile hardware and communication protocol are being pursued.

**KEYWORDS:** Optical detector readout concepts; Data acquisition circuits; Front-end electronics for detector readout; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases)

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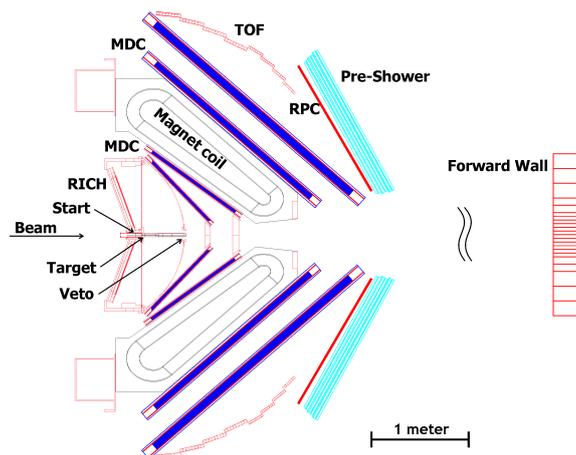
## 1 The HADES experiment

The High Acceptance Di-Electron Spectrometer (HADES) detector setup [1] is a high-acceptance magnetic spectrometer with a six-fold segmentation. A cross-section of the HADES detector is shown in figure 1. The detector is built with a minimal material budget in the inner detectors and high geometrical acceptance in both polar and azimuthal angles.

Charged particles are reconstructed based on their identification and their momentum measured by specific detectors. Their trajectory is determined by four layers of multi-wire drift chambers. Two are located in front of and two behind a superconducting toroidal magnet aligned with the beam axis. The deflection in the magnetic field gives the reconstruction of the momentum of the particle.

The identification of electrons is provided by a set of detectors. The first is a ring-imaging Cherenkov detector. The gas filled detector is sensitive to particles with a gamma factor  $> 18$ . In the reachable energy regime of the accelerator (SIS18), only electrons reach these velocities. Hence, the detector is blind for all kinds of hadrons. In particular, the pion suppression factor is in the order of  $10^3$ . Additional rejection power comes from the pre-Shower detector positioned in the lower polar angle region ( $15^\circ$ - $45^\circ$ ) in the outer part of the detector. Here, electrons/positrons are identified by the electromagnetic shower they produce when traversing two layers of lead plates.

The time-of-flight (TOF) detector consists of two parts: The inner part consists of resistive plate chambers (RPC) [2] which were installed during the recent upgrade phase as replacement of a low granularity scintillation detector (Tofino). The new detector consists of 1122 single-cell, 4-gap counters and has a time resolution well below 100 ps. The outer part of the time-of-flight wall consists of 64 scintillator strips per sector.



**Figure 1.** A cross section of the HADES spectrometer. From inner to outer, the detectors are the start and the veto diamond detectors, a ring imaging Cherenkov detector (RICH), four layers of multiwire drift chambers (MDC), a superconducting magnet, a time-of-flight wall (TOF), resistive plate chambers (RPC) and a pre-shower detector. A forward hodoscope is located 7 m downstream from the target (distance not to scale). For the sake of clarity only two of the six sectors are shown.

The spectrometer is further supplemented with a forward wall hodoscope covering polar angles below 7 degrees to detect fragments of beam particles. Two diamond detectors placed in front of and behind the target provide a reference time for the recorded events and are used to generate the trigger signals. In total, the HADES spectrometer comprises about 80,000 individual detector cells.

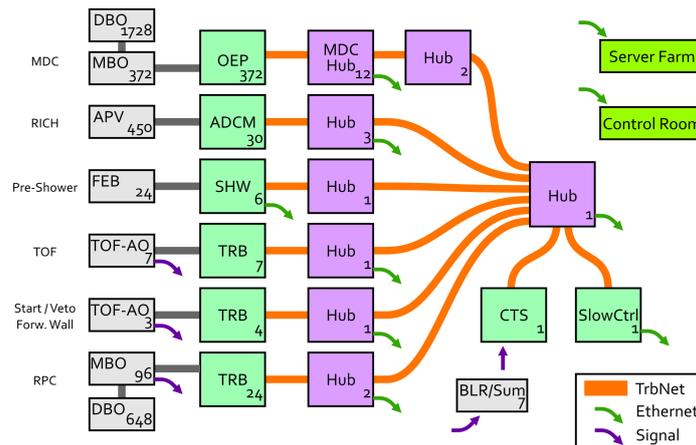
## 2 Description of the components

The HADES data acquisition system was originally designed and built ten years ago. The performance was sufficient for all experiments run in recent years, but does not meet the requirements for the planned experiments with heavy ions and higher beam energies at the FAIR<sup>1</sup> accelerator complex. Here, the data rate is of special concern since the mean particle multiplicities are increased by a factor 40 compared to light ion systems and data rates were already a limiting factor in these experiments. Hence, the DAQ system was re-designed based on new technologies to cope with the new requirements.

One central objective was to connect all sub-systems using a common network set-up to simplify development, integration and maintenance. Additionally, the control and monitoring features of the old systems had to be improved. Here, all electronics are based on platforms equipped with Field Programmable Gate Arrays (FPGA) and optical links. All data links run a dedicated network protocol, TrbNet, which is described in detail in the following section. A sketch of the complete DAQ system is given in figure 2.

As shown in the figure, the largest sub-system is the read-out for the MDC detector. Each front-end module consists of three parts: The signals from the detector are first amplified and discriminated by dedicated ASICs (ASD8). The time and amplitude (via time-over-threshold measurement) are digitized in Time-to-Digital Converters (TDC) with a time binning of 500 ps. Each

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**Figure 2.** The DAQ system. Data from analog front-ends are digitized by read-out controllers and forwarded over optical network running a dedicated protocol (TrbNet). Data are first combined from several front-ends and then forwarded to the server farm using Gigabit Ethernet. The whole system is controlled by the Central Trigger System (CTS). All nodes can also be accessed via a slow-control channel for configuration and monitoring.

of these front-ends connects 64 or 96 detector channels to the read-out controller. The read-out controller is equipped with a small FPGA (Lattice ECP2/M-20), an optical link (Firecomms FOT, 250 Mbit/s), voltage regulators and monitors as well as further components like Flash ROMs and level converters. The full read-out electronics of the MDC detector is described in [3] and [4].

One remarkable point is the very strict space constraint. In order to achieve a good measurement precision, all electronics have to be mounted on the frame of the chambers. Here, the space available for the read-out controller is  $4\text{ cm} \times 5\text{ cm}$  only. Additionally, the space to run cables out of the detector is limited so that all data communication to and from the read-out controller has to be implemented in a single fiber connection.

For the other sub-systems similar electronics has been developed. The front-end electronics (FEE) for the TOF and forward wall consists of the TRB2 TDC platform [5] and an AddOn to this board containing signal amplification, modification and shaping stages. The pre-Shower detector is controlled by a FPGA platform containing 96 ADC channels with 40 MSPS and 10 Bit resolution.

### 3 The DAQ network

The HADES DAQ network consists of two parts: An FPGA based custom network with optical links inside the detector and a commercial Gigabit Ethernet infrastructure transporting data to the server farm. The custom optical network features high bandwidth, low latency bi-directional data transport. All data are transported via this network on dedicated virtual channels: trigger information, event data and slow-control information. The two parts and three network channels are described in this section.

### 3.1 Network architecture

In a triggered read-out system, the data transport latency from the Central Trigger System (CTS) to the front-ends is of great importance. The round-trip time of trigger and busy release information defines the achievable trigger rates. The aim of the upgraded HADES DAQ is to reach up to 100 kHz trigger rate resulting in an allowed one-way latency of  $5 \mu\text{s}$ . Combined with the strict space constraints for the MDC system, no available network implementation met all requirements so that a custom network protocol, TrbNet, was designed.

The protocol combines three virtual channels for each of the different types of data into one network fiber. Inside the FPGAs, all channels are treated individually to keep interference between channels at a minimum. The data transported on the shared data transmission links has a high granularity with a packet size of 80 Bit. This allows the link arbiter to switch between channels almost immediately even while a transfer is running on another virtual channel. Typically, switching takes place within 100 ns to guarantee the shortest possible latency for trigger information

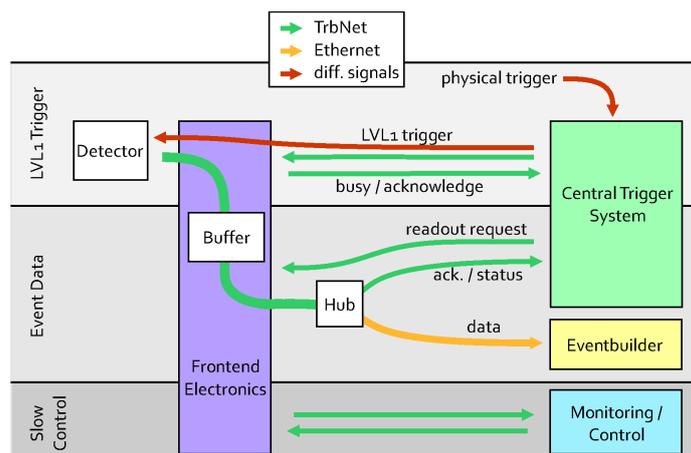
For each channel, several error detection and error prevention features are included. First, all data transferred has to be acknowledged by the receiver to prevent buffer overflows. Here, data is separated into blocks based on the buffer capacity of the receiver. Only two blocks of data are allowed to be sent before the transmitter has to wait for an acknowledge of the receiver which signals that the buffer space is available again. Further information about the data format and handshakes can be found in [6].

### 3.2 Trigger and readout process

Both the trigger and the read-out process are controlled by a central instance, the Central Trigger System (CTS). The CTS is supplied with fast input signals from different detector sub-systems. Based on these signals, a trigger decision is made. For each accepted trigger, first a reference time signal is sent to all front-ends via a dedicated differential link. The synchronization between all sub-systems is provided with an accuracy better than 30 ps event-to-event jitter. Second, a LVL1 trigger packet is sent over the optical network to all front-ends. It contains all necessary information to process the trigger, e.g. trigger type or event number. Here, also special trigger types for calibration and status information are implemented which are not preceded by a reference time signal. Upon a received trigger, the front-ends perform the read-out of the detector electronics and stores all data inside buffers. Typically, these buffers are able to store several hundred events before read-out has to take place.

The read-out sequence is again controlled by the CTS. It sends a request containing the event number and the server number to send data to. The front-ends fetch the event from the buffers and send it over the optical network. In network hubs, data from several front-ends is merged into one data stream, i.e. the event information sent by the front-ends is checked for validity, redundant information is stripped and all data is combined to one sub-event. Afterwards, the hub forwards the combined data stream to the next level of hubs for further combining.

For each sub-system there is one layer of network hubs (compare figure 2) in which data is extracted from TrbNet to be sent to the server farm via commercial Ethernet switches. First, data is packed into the HADES common event data structure. These converted data are then equipped with UDP and Ethernet headers and routed to the server farm. The decision which of the several servers



**Figure 3.** The TrbNet network is divided into three channels. The first one handles sending triggers from the Central Trigger System to the front-ends and busy-release information in the return path. Data are stored in the front-ends until a read-out request is received on the second channel. Data is then forwarded to hubs and converted to Gigabit Ethernet. The third channel handles all slow-control accesses.

receive the data is made by the CTS and distributed with the read-out request. The GbE interfaces contain a look-up table with all relevant information like IP and MAC addresses to provide the correct GbE headers.

### 3.3 Event building and data storage

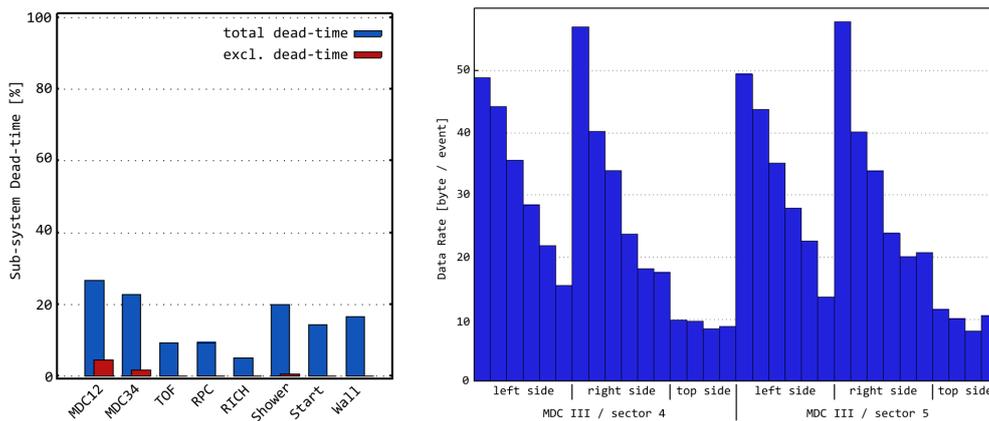
Inside the detector, all data is transported over the TrbNet links. Inside network hubs, data is extracted from the optical network and sent to the server farm (“Event Builders”) using the commercial Gigabit Ethernet standard. The GbE standard was chosen for several reasons: First, no special requirements are necessary in the path transporting pure data. Second, a GbE network can be built with off-the-shelf components, supports routing of data to different server nodes and the integration to all common hardware platforms is provided.

Most optical links in the data acquisition network run at 2 GBit/s link speed. The maximal available bandwidth is 150 MByte/s per link due to protocol overhead and 8b/10b encoding. The Gigabit Ethernet interfaces can send up to 50 MByte/s each to the event builders (an implementation with pipe-lining running at 100 MByte/s is under development).

The server farm consists of several high-performance servers with 12 CPU cores, 24 hard-disks (48 TB) and large memory (64 GB). On each machine, several event-builder processes receive asynchronous data streams from the various sub-systems and assemble them to complete events. Data are then written to local disk storage and forwarded to the GSI computing center for permanent storage and analysis.

### 3.4 Slow control

One central aspect of the new DAQ system is the possibility to control and monitor each front-end board individually. Hence, a versatile slow control functionality was implemented. Each module can be identified by the unique ID provided by a 1-wire temperature sensor. Based on this ID, a



**Figure 4.** Two examples of the on-line monitoring capabilities. Left: Dead-time of different sub-systems. Right: Data-rates of each front-end of two of the 24 drift-chambers. (Labels have been altered for better readability)

network address is assigned by software in a DHCP-like mechanism. These addresses do not only provide the access to individual front-ends but are also used to encode the position of front-ends boards within the detector inside the data and during analysis. Broadcast addresses to access all boards or sub-groups simultaneously are available as well.

Inside each network node, a 16 bit address bus provides the connection for every kind of control, status or debugging register and any kind of higher-level components. A standardized set of register available in all nodes further simplifies the monitoring of basic information about the full system.

Most boards provide the option to upgrade the FPGA design through the optical network. The design is stored in a flash chip which can be programmed remotely. Afterward, a reboot of the FPGA can be triggered. Some boards also offer a dual boot feature to prevent the risk of a memory corruption while upgrading the ROM. Interfaces to wide-spread protocols like SPI and I<sup>2</sup>C are available as well.

The computer interface for slow-control purposes is formed by a software library which gives the possibility to add software modules without coping with details of the network protocol. The library features both local access from the embedded Linux system on the TRB as well as remote, Ethernet based access from any other computer in the network. Figure 4 gives two examples of the monitoring capabilities of the DAQ system. Here, data is read from the front-ends via slow-control and visualized in real-time to give a fast overview on the status of the detector regarding dead-times and data-rates.

#### 4 August 2011 experimental run

In August 2011 an experimental run using a gold ion beam at an energy of 1.25 AGeV was performed. The beam was focussed on a 15-fold segmented gold foil target with an interaction rate of 1.5%. The beam intensity was  $2 \times 10^6$  ions per second, resulting in central gold-gold collisions

at 15 kHz rate. The DAQ system was able to record 10 kHz central events plus additional 3 kHz of peripheral collisions.

During the short run of 2.5 days, almost  $1 \times 10^9$  events amounting to 18 TB of data were recorded. The mean event size was 28 kByte resulting in a total data rate of 330 MByte/s. These data were distributed to eight event-builders (running on four physical machines) which wrote data to disk and forwarded them to the data storage center of GSI. The achieved trigger rate was about half of the projected rate of 20 kHz. Here, the limiting factors were both the beam intensity available from the accelerator and limits in the acceptable currents of the inner gas detectors. The event size was slightly higher than expected from simulation (26 kByte) due to the contribution of noise in the input signals.

One of the critical performance values is the latency to transport trigger information from the central trigger system to the front-ends. It has been measured to be in the range between  $1.9 \mu\text{s}$  in case of the RICH detector and  $4.7 \mu\text{s}$  for the MDC system. This difference is explained by an additional level of network hubs as well as the slower optical links used to connect the MDC front-ends.

## 5 Synergies and further improvements

Based on the developments for the HADES DAQ system, further hardware has been designed in cooperation with groups from other experiments. The experience with the TRB2 which is now used world-wide in many different applications, a next-generation TDC board has been built with sub-groups of the PANDA and CBM experiments. The TRB3 uses FPGA-based TDC circuits with a time resolution in the order of 10 ps, a high rate capability of 20 MHz per channel [7]. In total, the board is designed to house 256 TDC channels to allow a good integration in experiments with high channel count.

With its Add-On concept, the board can easily be adapted to any detector front-end and equipped with ADC or DAC channels as well as serial links or memory devices. The board itself consists of 5 large Lattice ECP3/150 FPGAs which provide huge logic resources for data pre-processing in four FPGAs. The fifth FPGA provides the necessary connectivity via 8 optical links capable of running various protocols including TrbNet and bi-directional Gigabit Ethernet for read-out and slow-control purposes.

The TrbNet protocol is also subject to further modifications. A second generation featuring higher performance and additional features is planned. The link speed will be increased to 3 Gbit/s and the protocol overhead for data transmission will be reduced to about 10%. The result will be an increase of 70% of the available bandwidth. Additional features include a global error detection and correction feature. On a per-link basis, check-sums will be added to the data stream and in case of an error the retransmission of a data packet can be requested. The synchronization of front-ends on the level of nanoseconds and a global clock distribution will also be integral part of the protocol. Additionally, an option for trigger-less systems is foreseen. Here, a regular time-stamping will generate data packets which are read out in a streaming mode.

## 6 Conclusion

We reported on the upgraded HADES DAQ system which was commissioned in 2011. The main approach was to use common electronics and common building blocks throughout all sub-systems to shorten development time and to ease later maintenance. This attempt has been proven to be very successful. It has been shown that integration of the network components into new hardware platforms can be accomplished in a very short time.

The measured network performance during the August 2011 experimental run meets or exceeds the requirements. An event rate of 68 kHz and a maximum data rate of 800 MByte/s was achieved under test conditions. During the experiment, data were collected at 15 kHz event rate and a data stream of 330 MByte/s. Here, the DAQ was not saturated and it can be assumed that both rates could be doubled.

The developed components and protocols are not only used in the HADES experiment, but are also employed by other experiments. The TRB2 read-out platform is in use world-wide by various groups. For example, the read-out of the prototype of the Micro-Vertex-Detector of the CBM experiment will be based on the TrbNet protocol and the TRB3 platform. The modular and configurable structure of all TrbNet components allows to easily adapt to the requirements of other experimental setups.

## Acknowledgments

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